Product Document

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TMD2636

Miniature Proximity Sensor Module

General Description

The TMD2636 features advanced proximity measurement in a tiny (1.0mm x 2.0mm) and extremely thin (0.35mm) optical land grid array module that incorporates a 940nm IR VCSEL and is factory calibrated for IR proximity response. The proximity detection feature provides object detection (e.g. close proximity) by photodiode detection of reflected IR energy sourced by the integrated VCSEL emitter. Detect/release events can be interrupt driven, and occur when proximity result crosses upper and/or lower threshold settings. The proximity engine features a wide range offset adjustment to compensate for unwanted IR energy reflection at the sensor. Proximity results are further improved by automatic ambient light subtraction.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TMD2636 Proximity Sensor Module are listed below:

Figure 1:
Added Value of Using TMD2636

Benefits	Features
• Optimized for small wearable devices	• Tiny 1.0mm x 2.0mm x 0.35mm module
• Reduced power consumption	• 1.8V power supply with 1.8V I^2C bus • Sleep mode (0.7µA) with fast wakeup • VCSEL IR emitter
• Enables superior proximity detection	• Integrated factory calibrated 940nm IR VCSEL • Crosstalk and ambient light cancellation • Wide configuration range
• Industrial design flexibility	• Dual photodiode architecture • Offset emitter/detector package design

Applications

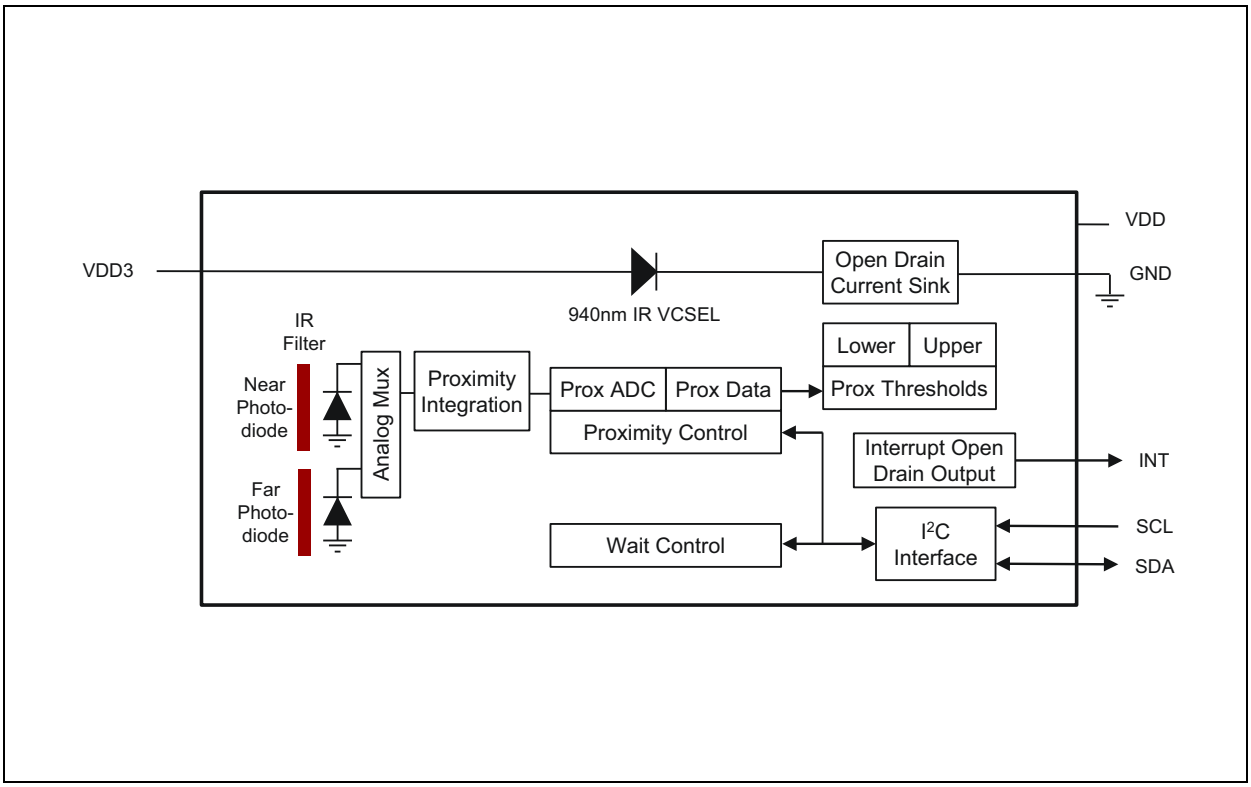
The TMD2636 applications for wearable products such as true-wireless stereo earbuds, glasses, and watches include:

- Power control (automatic power up/down based on user insertion/removal)
- Volume/mode control user detection (up/down/mute based on user touch/tap)

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of TMD2636



Pin Assignment

Device pinout is described below.

Figure 3:
Pin Diagram of TMD2636 (Top View)

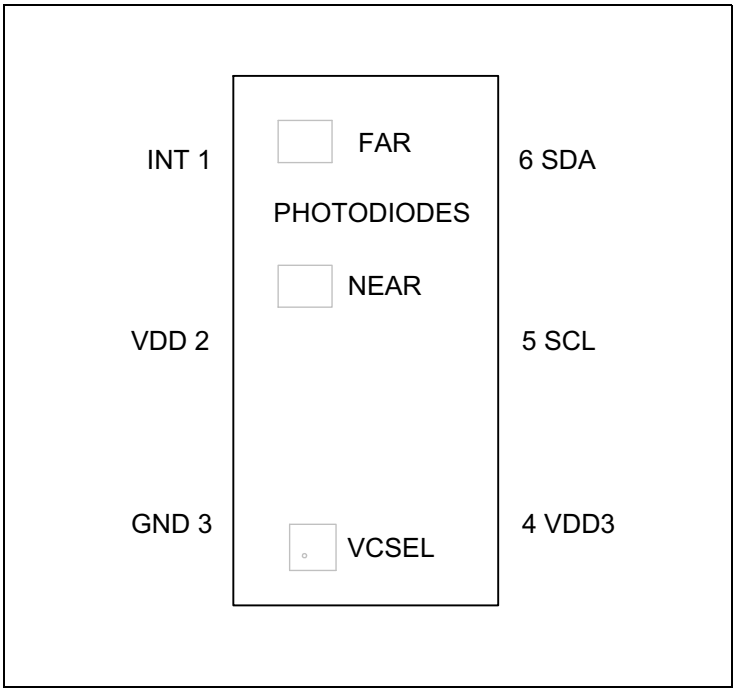


Figure 4:
Pin Description

Pin Number	Pin Name	Description
1	INT	Interrupt. Open drain output (active low). If INT is not used, tie to GND for enhanced ESD protection.
2	VDD	Supply voltage for sensor (1.8V). To enable the device to recover from a high voltage system ESD strike, it is recommended to connect VDD to a host GPIO pin for independent power control.
3	GND	Ground. All voltages are referenced to GND.
4	VDD3	Supply voltage for IR emitter (3.0/3.3V)
5	SCL (1)	I^2C serial clock input terminal
6	SDA (1)	I^2C serial data I/O terminal

Note(s):

1. When the SDA and SCL signals are swapped, the device uses a different I^2C address. See the I^2C Characteristics section for more details.

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
VDD	Supply voltage to GND	-0.3	2.0	V	
VDD3	IR emitter voltage to GND	-0.3	3.6	V	
V_{IO}	Digital I/O terminal voltage	-0.3	3.6	V	
I_{IO}	Digital output terminal voltage	-1	20	mA	
I_{SCR}	Input current (latch up immunity)	±100		mA	Class II JEDEC JESD78E
ESD_{HBM}	HBM Electrostatic discharge	±2000		V	JEDEC/ ESDA JS-001-2017
ESD_{CDM}	CDM Electrostatic discharge	±500		V	JEDEC JS-002-2018
T_{STRG}	Storage temperature range	-40	85	℃	
T_{BODY}	Package body temperature		260	°C	IPC/JEDEC J-STD-020 (1)
RH_{NC}	Relative humidity (non- condensing)	5	85	%	
P_{DISS}	Power dissipation		50	mW	Average power dissipation over a 1 second period

Note(s):

1. The reflow peak soldering temperature (body temperature) is specified according to IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices."

Electrical Characteristics

All limits are guaranteed. The parameters with min. and max. values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
VDD	Supply voltage to sensor	1.7	1.8	2.0	V
VDD3	Supply voltage to IR emitter	2.9	3.3	3.6	V
P_{DISS}	Average power dissipation (1)			20	mW
T_A	Operating ambient temperature	-30		85	°C

Note(s):

1. Power dissipation averaged over 1 second period.

Figure 7:
Operating Characteristics, VDD = 1.8 V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{OSC}	Oscillator frequency		7.9	8.1	8.3	MHz
I_{DD}	Supply current (1)	Active state (PON=1) (2)	197	340	482	µA
		Idle state (PON=1) (3)		30		
		Sleep state (PON = 0) (4)		0.7		
V_{OL}	INT, SDA output low voltage	6 mA sink current			0.6	V
I_{LEAK}	Leakage current, SDA, SCL, INT		-5		5	µA
V_{IH}	SCL, SDA input high voltage (5)		1.26			V
V_{IL}	SCL, SDA input low voltage				0.54	V
T_{Wakeup}	Time for device to wakeup from the sleep state and enter the active state if both PON and PEN are set to one at the same time.			100		µs
T_{Active}	Time from power-on to ready to receive I^2C commands			1.5		ms

Note(s):

1. Values are shown at the VDD pin and do not include current through the IR VCSEL.
2. Active state occurs when PON = 1 and the device is actively integrating. This time is determined by the number of pulses (PPULSE) and the pulse length (PULSE_LEN) according to the formula: (7 x PULSE_LEN) + PPULSE x (2 x PULSE_LEN + 22µs) + 78.75µs.

3. Idle state occurs when PON = 1 and the device is not in the active state.
4. Sleep state occurs when PON = 0 and I^2C bus is idle. If sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.
5. Digital pins: SDA, SCL, INT are tolerant to a communication voltage up to 3.4V.

Figure 8:
Near Proximity Photodiode Optical Characteristics, VDD = 1.8V, VDD3 = 3.0V, T_A = 25°C (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
Response: Absolute (1)	PGAIN = 1x PLDRIVE = 7mA PPULSE = 5 pulses PPULSE_LEN = 12µs APC = Disabled TEST9 = 0x07 BINSRCH_TARGET = 31 Post Calibration Target Material: 18% reflective surface No glass above module Target Size: 100mm x 100mm Target Distance: 10mm	283	377	471	Counts
Part to Part Variation (1) (2)	Same as Response: Absolute			±25	%
Noise (1) (2)	Same as Response: Absolute			±2	%
Response: No target (1) (3)	Same as Response: Absolute except no target above the module	19	30	41	Counts

Note(s):

1. Representative result by characterization.
2. 3 sigma (σ) variation.
3. Response with no target varies with power supply characteristics and system noise.

Figure 9:
Far Proximity Photodiode Optical Characteristics, VDD = 1.8V, VDD3 = 3.0V, T_A = 25°C (unless otherwise noted)

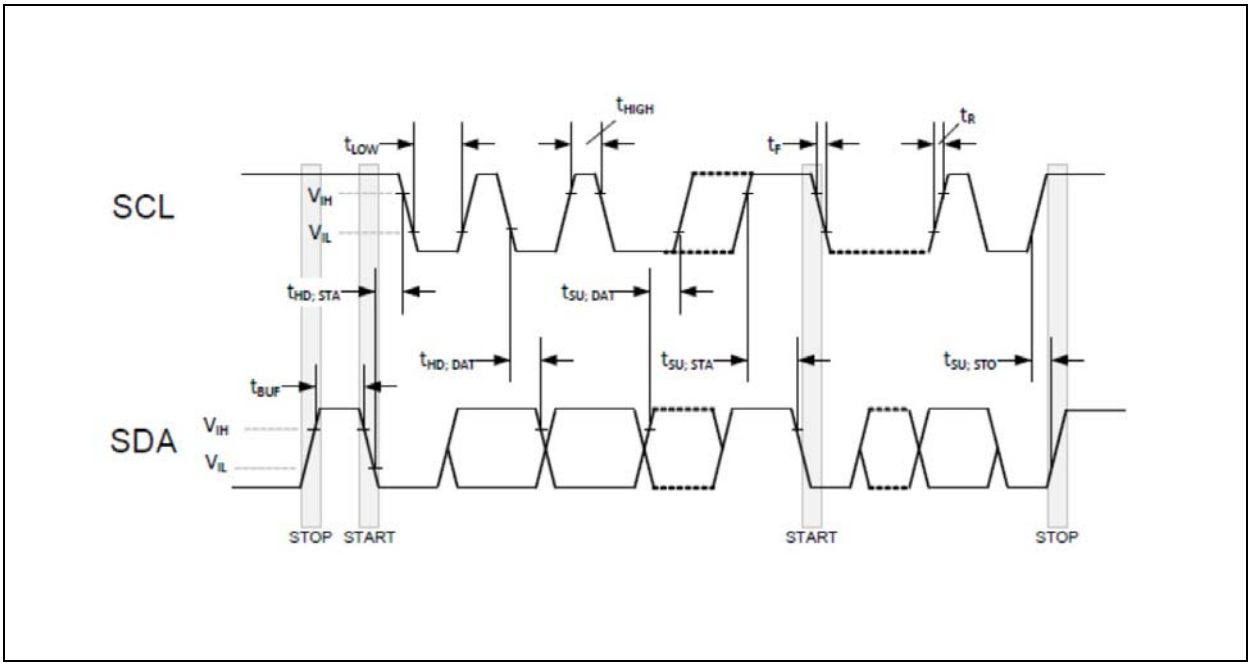
Parameter	Conditions	Min	Typ	Max	Unit
Response: Absolute (1)	PGAIN = 1x PLDRIVE = 7mA PPULSE = 5 pulses PPULSE_LEN = 12µs APC = Disabled TEST9 = 0x07 BINSRCH_TARGET = 31 Post Calibration Target Material: 18% reflective surface No glass above module Target Size: 100mm x 100mm Target Distance: 10mm	247	329	411	Counts
Part to Part Variation (1) (2)	Same as Response: Absolute			±25	%
Noise (1) (2)	Same as Response: Absolute			±2	%
Response: No target (1) (3)	Same as Response: Absolute except no target above the module	19	30	41	Counts

Note(s):

1. Representative result by characterization.
2. 3 sigma (σ) variation.
3. Response with no target varies with power supply characteristics and system noise.

Timing Characteristics

Figure 10:
I²C Timing Diagrams For TMD2636



Detailed Description

Proximity Operation

By varying gain, VCSEL drive current, number of VCSEL pulses and VCSEL pulse duration the proximity detection range can be adjusted.

Proximity

Proximity results are affected by three fundamental factors: the integrated IR VCSEL emission, IR reception, and environmental factors, including target distance and surface reflectivity. The IR reception signal path begins with IR detection from a photodiode and ends with the 14-bit proximity result in PDATA register. Signal from the photodiode is amplified, and offset adjusted to optimize performance. Offset correction or cross-talk compensation is accomplished by adjustment to the POFFSET register. The analog circuitry of the device applies the offset value as a subtraction to the signal accumulation; therefore a positive offset value has the effect of decreasing the results.

I²C Characteristics

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and fast clock frequency modes with a chip address of 0x39. Read and write transactions comply with the standard set by Philips (now NXP).

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP command and the I²C bus is released). During consecutive read transactions, the future/repeated I²C read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address + 1.

Alternate I²C Address Option

If the SDA and SCL pins are swapped as shown below, the device will switch to an alternate I²C address. This allows two devices to reside on the same bus. After power is applied to the devices, a single dummy I²C access (read or write with valid I²C stop) to any address or device on the same bus is required to initialize the devices to their respective I²C addresses. The devices will generate an NOT-ACKNOWLEDGE (NACK) during this initial dummy access.

Figure 11:
I²C Schemes

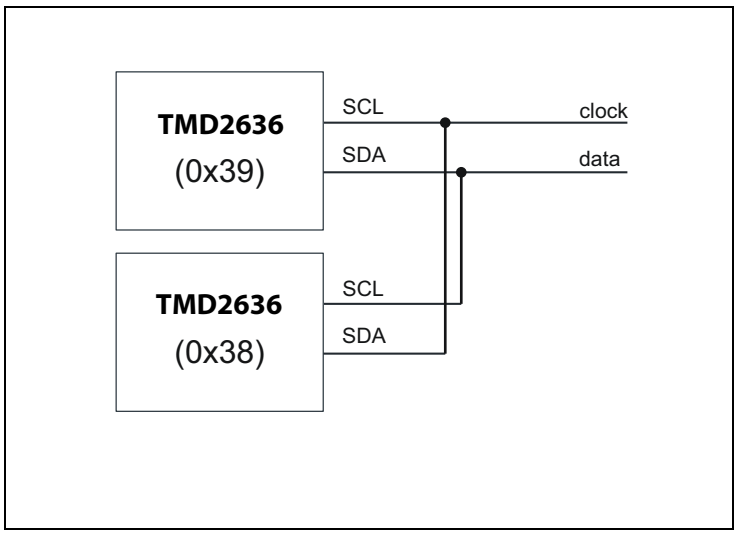


Figure 12:
I²C Address Selection

Master I²C Bus Signal		
Clock	Data	7-Bit I²C Address
SCL	SDA	0x39
SDA	SCL	0x38

I²C Write Transaction

A write transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS, DATA BYTE(S), and STOP. Following each byte (9^{th} clock pulse) the slave places an ACKNOWLEDGE/ NOT-ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

I²C Read Transaction

A Read transaction consists of a START, CHIP-$ADDRESS_{WRITE}$, REGISTER-ADDRESS, START, CHIP-$ADDRESS_{READ}$, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9^{th} clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

Alternately, if the previous I²C transaction was a read, the internal register address buffer is still valid, allowing the transaction to proceed without “re”-specifying the register address. In this case the transaction consists of a START, CHIP-ADDRESSREAD, DATA BYTE(S), and STOP. Following all but

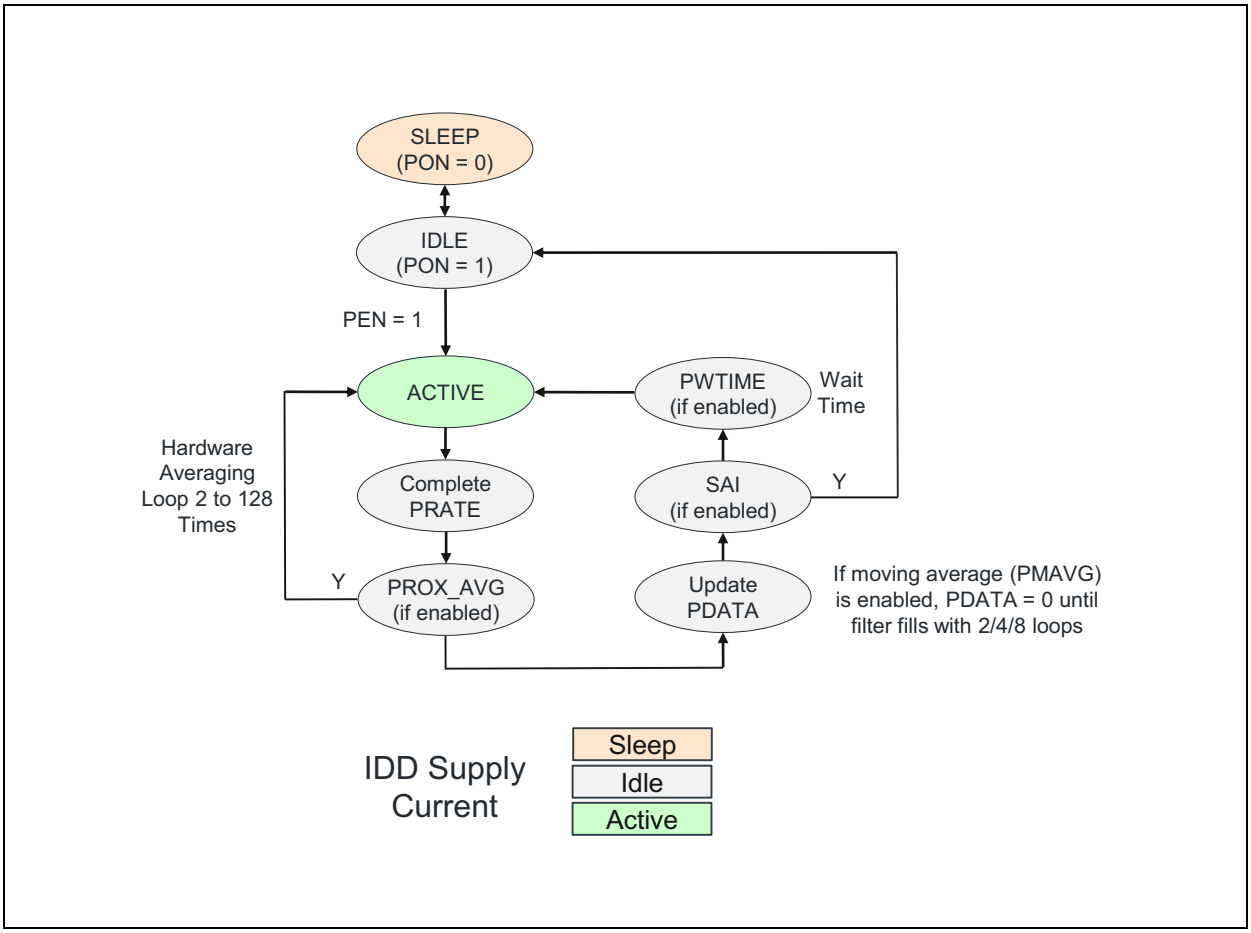
the final byte the master places an ACK on the bus (9th clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

The I²C bus protocol was developed by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification at:

http://www.i2c-bus.org/references/

Simplified State Diagram

Figure 13:
Simplified State Diagram



Register Description

Figure 14:
Register Overview

Address	Register Name	R/W	Register Function	Reset Value
0x80	ENABLE	R/W	Enables states and interrupts	0x00
0x82	PRATE	R/W	Proximity time	0x1F
0x88	PILTL	R/W	Proximity interrupt low threshold low byte	0x00
0x89	PILTH	R/W	Proximity interrupt low threshold high byte	0x00
0x8A	PIHTL	R/W	Proximity interrupt high threshold low byte	0x00
0x8B	PIHTH	R/W	Proximity interrupt high threshold high byte	0x00
0x8C	PERS	R/W	Proximity interrupt persistence filters	0x00
0x8D	CFG0	R/W	Configuration zero	0x40
0x8E	PCFG0	R/W	Proximity configuration zero	0x8F
0x8F	PCFG1	R/W	Proximity configuration one	0x60
0x91	REVID	R	Revision ID	0x10
0x92	ID	R	Device ID	0x44
0x9B	STATUS	R, SC	Device status	0x00
0x9C	PDATAL	R	Proximity ADC low data	0x00
0x9D	PDATAH	R	Proximity ADC high data	0x00
0xA6	REVID2	R	Revision ID two	0x03 or 0x0C
0xA8	SOFTRST	R/W	Soft reset	0x00
0xA9	PWTIME	R/W	Proximity wait time	0x00
0xAA	CFG8	R/W	Configuration eight	0x02
0xAB	CFG3	R/W	Configuration three	0x04
0xAE	CFG6	R/W	Configuration six	0x3F
0xB3	PFILTER	R/W	Proximity filter	0x00
0xC0	POFFSETL	R/W	Proximity offset low data	0x00
0xC1	POFFSETH	R/W	Proximity offset high data	0x00
0xD7	CALIB	R/W	Proximity offset calibration	0x00
0xD9	CALIBCFG	R/W	Proximity offset calibration control	0x50
0xDC	CALIBSTAT	R	Proximity offset calibration status	0x00

Address	Register Name	R/W	Register Function	Reset Value
0xDD	INTENAB	R/W	Interrupt enables	0x00
0xE5	FAC_L	R	Factory data low (lot code data)	0x00 to 0xFF
0xE6	FAC_H	R	Factory data high (lot code data)	0x00 to 0xFF
0xF9	TEST9	R/W	Test nine (must be set to 0x07)	0x00

Note(s):

1. R = Read Only, W = Write Only, R/W = Read or Write, SC = Self Clearing after access

ENABLE Register (0x80)

Figure 15:
ENABLE Register

Addr: 0x80		ENABLE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	Reserved	000	RW	Reserved. Must be set to default value
4	PWEN	0	RW	This bit activates the proximity wait feature which is set by the PWTIME register. Active high.
3	Reserved	0	RW	Reserved. Must be set to default value
2	PEN	0	RW	This bit activates the proximity detection. Active high.
1	Reserved	0	RW	Reserved. Must be set to default value
0	PON	0	RW	This field activates the internal oscillator and ADC channel. Active high.

Before activating PEN, preset each applicable operating mode register and bits.

PRATE Register (0x82)

Figure 16:
PRATE Register

Addr: 0x82		PRATE		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PRATE	0x1F	RW	This register defines the duration of 1 proximity sample, which is (PRATE + 1)*88µs.

PILTL Register (0x88)

Figure 17:
PILTL Register

Addr: 0x88		PILTL		
Bit	Bit Name	Default	Access	Bit Description
7:0	PILTL	0x00	RW	This register contains the low byte of the 14-bit proximity LOW threshold when APC is enabled. If APC is disabled, this register contains the LOW threshold which is an 8-bit value which is compared against the upper 8 bits of the 10-bit proximity value.

PILTH Register (0x89)

Figure 18:
PILTH Register

Addr: 0x89		PILTH		
Bit	Bit Name	Default	Access	Bit Description
7:6	Reserved	00	RW	Reserved. Must be set to default value.
5:0	PILTH	0x00	RW	This register contains the upper 6 bits of the 14-bit proximity LOW threshold when APC is enabled. If APC is disabled, this register is ignored.

The contents of the PILTH and PILTL registers are combined and treated as a fourteen (14) bit threshold low value. If the value generated by the proximity ADC (PDATA) is below the PILTL/H threshold and the PPERS value is reached, then the low proximity threshold is breached. When setting the 14-bit proximity threshold, PILTL must be written first, immediately follow by PILTH. Internally, the lower 8 bits are buffered until the upper 8 bits are written. As the upper 8 bits are written both the high and low bytes are simultaneously latched as a 14-bit value.

If Automatic Pulse Control (APC) is disabled by setting bit 6 in CFG6 to 1, then the proximity data converts to a 10-bit value. PILTL contains an 8-bit threshold which is compared against the upper 8 bits of the 10-bit value. PILTH is ignored.

PIHTL Register (0x8A)

Figure 19:
PIHTL Register

Addr: 0x8A		PIHTL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PIHTL	0x00	RW	This register contains the low byte of the 14-bit proximity HIGH threshold when APC is enabled. If APC is disabled, this register contains the HIGH threshold which is an 8-bit value which is compared against the upper 8 bits of the 10-bit proximity value.

PIHTH Register (0x8B)

Figure 20:
PIHTH Register

Addr: 0x8B		PIHTH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Reserved	00	RW	Reserved. Must be set to default value.
5:0	PIHTH	0x00	RW	This register contains the upper 6 bits of the 14-bit proximity HIGH threshold when APC is enabled. If APC is disabled, this register is ignored.

The contents of the PIHTH and PIHTL registers are combined and treated as a fourteen (14) bit threshold high value. If the value generated by the proximity ADC (PDATA) is above the PIHTL/H threshold and the PPERS value is reached, then the high proximity threshold is breached. When setting the 14-bit proximity threshold, PIHTL must be written first, immediately follow by PIHTH. Internally, the lower 8 bits are buffered until the upper 8 bits are written. As the upper 8 bits are written both the high and low bytes are simultaneously latched as a 14-bit value.

If Automatic Pulse Control (APC) is disabled by setting bit 6 in CFG6 to 1, then the proximity data converts to a 10-bit value. PIHTL contains an 8-bit threshold which is compared against the upper 8 bits of the 10-bit value. PIHTH is ignored.

PERS Register (0x8C)

Figure 21:
PERS Register

Addr: 0x8C		PERS		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0 (0000)	RW	Reserved. Must be set to default value.
3:0	PPERS	0 (0000)	RW	This register sets the proximity persistence filter.

Value	Interrupt
0 (0000)	Every proximity cycle
1 (0001)	Any value outside proximity thresholds
2 (0010)	2 consecutive proximity values out of range
3 (0011)	3 consecutive proximity values out of range
...	...
15 (1111)	15 consecutive proximity values out of range

The frequency of consecutive proximity channel results outside of threshold limits are counted; this count value is compared against the PPERS value. If the counter is equal to the PPERS value an interrupt is asserted. Any time a proximity channel result is inside the threshold values the counter is cleared.

CFG0 Register (0x8D)

Figure 22:
CFG0 Register

Addr: 0x8D		CFG0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0100	RW	Reserved. Must be set to default value.
3	PWLONG	0	RW	When PWLONG (PROX Wait Long) is asserted the wait period as set by PWTIME is increased by a factor of 12.
2:0	Reserved	000	RW	Reserved. Must be set to default value.

PCFG0 Register (0x8E)

Figure 23:
PCFG0 Register

Addr: 0x8E		PCFG0			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:6	PGAIN	2 (10)	RW	This field sets the gain of the proximity IR sensor.	
				Value	**Gain**
				0 (00)	1x
				1 (01)	2x
				2 (10)	4x
				3 (11)	8x
5:0	PPULSE	15 (001111)	RW	Maximum number of pulses in a single proximity cycle.	
				Value	**Maximum Number of Pulses**
				0 (00000)	1
				1 (00001)	2
				2 (00010)	3
				...	...
				63 (11111)	64

The PPULSE field sets the maximum number of IR VCSEL pulses that may occur in a proximity cycle. The proximity engine will automatically continue to add IR VCSEL pulses, up to the value set in PPULSE or if a near-saturation condition occurs if Automatic Pulse Control (APC) is enabled. The dynamic range of the sensor is automatically adjusted to detect distant targets as well as prevent saturation from close targets. This operation also reduces power consumption because proximity integration period is automatically shortened when a target is close to the sensor.

If Automatic Pulse Control (APC) is disabled by setting bit 6 in CFG6 to 1, then PPULSE always determines the number of proximity pulses to be transmitted.

PCFG1 Register (0x8F)

Figure 24:
PCFG1 Register

Addr: 0x8F		PCFG1			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:5	PPULSE_LEN	3 (011)	RW	Proximity pulse length.	
				Value	**Pulse Length**
				0 (000)	1µs
				1 (001)	2µs
				2 (010)	4µs
				3 (011)	8µs
				4 (100)	12µs
				5 (101)	16µs
				6 (110)	24µs
				7 (111)	32µs
4	Reserved	0	RW	Reserved. Must be set to default value	
3:0	PLDRIVE	0 (0000)	RW	This field sets the drive strength of the IR VCSEL current. Values are approximate; actual current through VCSEL is factory trimmed to normalize IR intensity. For lowest part to part variation, 7mA is recommended.	
				Value	**VCSEL Current**
				5 (0101)	7mA
				6 (0110)	8mA
				7 (0111)	9mA
				8 (1000)	10mA
				All other values	Reserved

The PPULSE_LEN field sets the length (width) of all IR VCSEL pulses within the proximity cycle. Longer pulses result in increased proximity range and typically result in less electrical noise generated in the analog front end.

REVID Register (0x91)

Figure 25:
REVID Register

Addr: 0x91		REVID		
Bit	Bit Name	Default	Access	Bit Description
7:3	Reserved	00010	RO	Reserved
2:0	REV_ID	000	RO	Device revision number

ID Register (0x92)

Figure 26:
ID Register

Addr: 0x92		ID		
Bit	Bit Name	Default	Access	Bit Description
7:2	ID	010001	RO	Device type identification
1:0	Reserved	00	RO	Reserved

STATUS Register (0x9B)

Figure 27:
STATUS Register

Addr: 0x9B		STATUS		
Bit	Bit Name	Default	Access	Bit Description
7	PHIGH	0	R, SC	Set when PINT is set and PDATA > high threshold (after persistence). Cleared when PINT is cleared.
6	PLOW	0	R, SC	Set when PINT is set and PDATA < low threshold (after persistence). Cleared when PINT is cleared.
5	PSAT	0	R, SC	Proximity saturation flag indicates that an ambient or reflective-saturation event occurred during a previous proximity cycle.
4	PINT	0	R, SC	Proximity interrupt flag indicates that proximity results have exceeded thresholds and persistence settings.
3	CINT	0	R, SC	Calibration interrupt flag indicates that calibration has completed.
2	ZINT	0	R, SC	Zero detection interrupt flag indicates that a zero value in PDATA has caused the proximity offset to be decremented (if AUTO_OFFSET_ADJ = 1).
1	PSAT_ REFLECTIVE	0	R, SC	The Reflective Proximity Saturation Interrupt flag signals that the AFE has saturated during the IR VCSEL active portion of proximity integration.
0	PSAT_ AMBIENT	0	R, SC	The Ambient Proximity Saturation Interrupt flag signals that the AFE has saturated during the IR VCSEL inactive portion of proximity integration.

All flags in this register can be cleared by setting the bit high. Alternatively, if the INT_READ_CLEAR in the CFG3 register bit is set, then simply reading this register automatically clears all eight flags.

PDATAL Register (0x9C)

Figure 28:
PDATAL Register

Addr: 0x9C		PDATAL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PDATAL	0x00	RO	This register contains the low byte of the 14-bit proximity ADC data when APC is enabled. If APC is disabled, this register contains the upper 8 most significant bits of the 10-bit proximity value.

PDATAH Register (0x9D)

Figure 29:
PDATAH Register

Addr: 0x9D		PDATAH		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	PDATAH	0x00	RO	This register contains the high byte of the 14-bit proximity ADC data when APC is enabled. If APC is disabled, bits 1:0 contain the lower 2 bits of the 10-bit proximity value.

Proximity data is stored as a 14-bit value (two bytes). Reading the low byte first latches the high byte. Proximity detection uses an Automatic Pulse Control (APC) mechanism that adjusts the number of pulses per measurement based on the magnitude of the reflected IR signal. As the magnitude of the signal increases, the number of pulses decreases. Proximity detection uses a 10-bit ADC that is extended to a 14-bit dynamic range for PDATA using the following formula:

$PDATA = ADC_{value} \times (16 / \text{actual number of pulses transmitted})$

PDATA is therefore proportional to the reflected energy independent of the number of pulses transmitted.

If Automatic Pulse Control (APC) is disabled by setting bit 6 in CFG6 to 1, then the proximity data converts to a 10-bit value. PDATAL contains the 8 most significant bits of the 10-bit value and PDATAH bit locations 1:0 contain the lower 2 bits. When APC is disabled, only the upper 8 bits are compared against the threshold values contained in PILTL and PIHTL.

REVID2 Register (0xA6)

Figure 30:
REVID2 Register

Addr: 0xA6		REVID2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reserved	0000	RO	Reserved
3:0	VER_ID	0011 or 1100	RO	Device version number

SOFTRST Register (0xA8)

Figure 31:
SOFTRST Register

Addr: 0xA8		SOFTRST		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:1	Reserved	0000000	RW	Reserved. Must be set to default value.
0	SOFTRST	0	RW	Writing a 1 to this bit will cause all registers to be reset to their default state. This will immediately terminate all device operation and put the device into the sleep state.

PWTIME Register (0xA9)

Figure 32:
PWTIME Register

Addr: 0xA9		PWTIME				
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**		
7:0	PWTIME	0x00	RW	Value that specifies the wait time in 2.78ms increments.		
				Value	**Increment**	**Wait Time**
				0x00	1	2.78ms (33.4ms)
				0x01	2	5.56ms (66.7ms)
				0x11	18	50.0ms (600ms)
				0x23	36	100ms (1.20s)
				0x3F	64	178ms (2.14s)
				0xFF	256	712ms (8.54s)

The wait timer is implemented using a down counter.
Wait time = increment x 2.78ms. If PWLONG is enabled (bit 3 in CFG0), then wait time = increment x 2.78ms x 12

CFG8 Register (0xAA)

Figure 33:
CFG8 Register

Addr: 0xAA		CFG8			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:2	Reserved	000000	RW	Reserved. Must be set to default value.	
1:0	PDSELECT	10	RW	Proximity photodiode selection	
				Value	**Photodiode Selected**
				00	No photodiode
				01	Far photodiode
				10	Near photodiode (default)
				11	Both photodiodes

CFG3 Register (0xAB)

Figure 34:
CFG3 Register

Addr: 0xAB		CFG3					
Bit	Bit Name	Default	Access	Bit Description			
7	INT_READ_CLEAR	0	RW	If set, then flag bits in the STATUS register will be reset whenever the STATUS register is read over I^2C.			
6:5	Reserved	00	RW	Reserved. Must be set to default value.			
4	SAI	0	RW	The sleep after interrupt bit is used to place the device into a low power mode upon an interrupt pin assertion.			
				PON	**SAI**	**INT**	**Oscillator**
				0	X	X	OFF
				1	0	X	ON
				1	1	1	ON
				1	1	0	OFF
3:0	Reserved	0100	RW	Reserved. Must be set to default value.			

The SAI bit sets the device operational mode following the completion of a proximity cycle. If PINT and PIEN are both set, causing an interrupt on the INT pin, and the SAI bit is set, then the oscillator will deactivate. The device will appear as if PON = 0, however, PON will read as 1. The device can only be reactivated (oscillator enabled) by clearing the interrupts in the STATUS register.

CFG6 Register (0xAE)

Figure 35:
CFG6 Register

Addr : 0xAE		CFG6		
Bit	Bit Name	Default	Access	Bit Description
7	Reserved	0	RW	Reserved. Must be set to default value.
6	APC_DISABLE	0	RW	Proximity automatic pulse control (APC) disable. 0 = APC enable 1 = APC disable
5:0	Reserved	111111	RW	Reserved. Must be set to default value.

PFILTER Register (0xB3)

Figure 36:
PFILTER Register

Addr: 0xB3		PFILTER		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	Reserved	000000	RW	Reserved. Must be set to default value.
1:0	PMAVG	00	RW	Proximity moving average

Value	Proximity Moving Average
00	Disabled (default)
01	2 values
10	4 values
11	8 values

The PMAVG bits select the moving average that is performed on the proximity data before it is loaded into PDATA and checked against the thresholds. The moving average uses data after proximity hardware averaging is performed (refer to the PROX_AVG bits in the CALIBCFG register).

POFFSETL Register (0xC0)

Figure 37:
POFFSETL Register

Addr: 0xC0		POFFSETL		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	POFFSETL	0x00	RW	This register contains the magnitude portion of proximity offset adjust value.

POFFSETH Register (0xC1)

Figure 38:
POFFSETH Register

Addr: 0xC1		POFFSETH		
Bit	Bit Name	Default	Access	Bit Description
7:1	Reserved	0000000	RW	Reserved. Must be set to default value.
0	POFFSETH	0	RW	This register contains the sign portion of proximity offset adjust value.

Typically, optical and/or electrical crosstalk negatively influence proximity operation and results. The POFFSETL/POFFSETH registers provide a mechanism to remove system crosstalk from the proximity data. POFFSETL and POFFSETH contains the magnitude and sign of a value which adjusts PDATA is generated in the AFE. An offset value in the range of ± 255 is possible.

CALIB Register (0xD7)

Figure 39:
CALIB Register

Addr: 0xD7		CALIB		
Bit	Bit Name	Default	Access	Bit Description
7	CALAVG	0	RW	Enables proximity hardware averaging as selected with PROX_AVG during calibration. 0 = No hardware averaging 1 = Hardware averaging enabled
6	Reserved	0	RW	Reserved. Must be set to default value.
5	ELECTRICAL_ CALIBRATION	0	RW	Selects proximity calibration type. 0 = Electrical and optical crosstalk. 1 = Electrical crosstalk only.
4	CALPRATE	0	RW	Enables PRATE during calibration. Useful when averaging is enabled. 0 = PRATE ignored 1 = PRATE applied between averaging samples
3:1	Reserved	000	RW	Reserved. Must be set to default value.
0	START_ OFFSET_CAL	0	RW	Set to 1 to start a calibration sequence.

Proximity response in systems with electrical and optical crosstalk may be improved by using the calibration feature. Optical crosstalk is caused when the photodiode receives a portion of the VCSEL IR which was unintentionally reflected by a surface other than the target. Electrical offset is caused by electrical disturbance in the sensor AFE, and also influences the proximity result. The calibration routine adjusts the value in POFFSETL/H until the proximity result is as close to the binary search target as possible. Optical and electrical calibration function identically, except that during an electrical calibration the proximity photodiode is disconnected from the AFE.

An electrical calibration can be initiated anytime by setting the ELECTRICAL_CALIBRATION and START_OFFSET_CAL bits. To perform an optical (and electrical) calibration do not set the ELECTRICAL_CALIBRATION bit when setting the START_OFFSET_CALIB. The CINT flag will assert after calibration has finished. Upon completion proximity offset registers are automatically loaded with calibration result.

CALIBCFG Register (0xD9)

Figure 40:
CALIBCFG Register (0xD9)

Addr: 0xD9		CALIBCFG			
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**	
7:5	BINSRCH_ TARGET	2 (010)	RW	Proximity offset calibration result target	
				Value	**PDATA Target**
				0 (000)	3
				1(001)	7
				2 (010)	15
				3 (011)	31
				4 (100)	63
				5 (101)	127
				6 (110)	255
				7 (111)	511
4	Reserved	1	RW	Reserved. Must be set to default value.	
3	AUTO_OFFSET_ ADJ	0	RW	If set, this bit causes the value in POFFSETL register to be decremented if PDATA ever becomes zero.	

<table>
<tr><th colspan="2">Addr: 0xD9</th><th colspan="3">CALIBCFG</th></tr>
<tr><th>Bit</th><th>Bit Name</th><th>Default</th><th>Access</th><th>Bit Description</th></tr>
<tr><td rowspan="9">2:0</td><td rowspan="9">PROX_AVG</td><td rowspan="9">0
(000)</td><td rowspan="9">RW</td><td colspan="2">PROX_AVG defines the number of ADC samples collected and hardware averaged during a proximity cycle.</td></tr>
<tr><td>Value</td><td>Sample Size</td></tr>
<tr><td>0 (000)</td><td>Disable</td></tr>
<tr><td>1 (001)</td><td>2</td></tr>
<tr><td>2 (010)</td><td>4</td></tr>
<tr><td>3 (011)</td><td>8</td></tr>
<tr><td>4 (100)</td><td>16</td></tr>
<tr><td>5 (101)</td><td>32</td></tr>
<tr><td>6 (110)</td><td>64</td></tr>
<tr><td>7 (111)</td><td>128</td></tr>
</table>

The binary search target field is used by the calibration feature to set the baseline value for PDATA when no target is present. For example, calibration of a device in open air, with no target, and BINSEARCH_TARGET setting of 2 causes the PDATA value will be approximately 15 counts. This feature is useful because it forces PDATA result to always be above zero.

The PROX_AVG field sets the number of ADC samples that are averaged. Each ADC sample causes the programmed number of proximity pulses to be transmitted. Once all samples have been completed and the average is calculated, the proximity state machine will then pass this value either directly to PDATA or to the proximity moving average filter depending on the configuration of the PMAVG bits in the PFILTER register.

CALIBSTAT Register (0xDC)

Figure 41:
CALIBSTAT Register

Addr: 0xDC		CALIBSTAT		
Bit	Bit Name	Default	Access	Bit Description
7:3	Reserved	00000	RW	Reserved. Must be set to default value.
2	OFFSET_ ADJUSTED	0	RW	Bit is set when the proximity offset has been automatically decremented if AUTO_OFFSET_ADJ = 1 (see CALIBCFG register). This bit can be cleared by writing 1 to it or setting AUTO_OFFSET_ADJ to 0.
1	Reserved	0	RW	Reserved. Must be set to default value.
0	CALIB_FINISHED	0	RW	This flag indicates that calibration has finished. This bit is a copy of the CINT bit in the STATUS register. It will be cleared when the CINT bit is cleared.

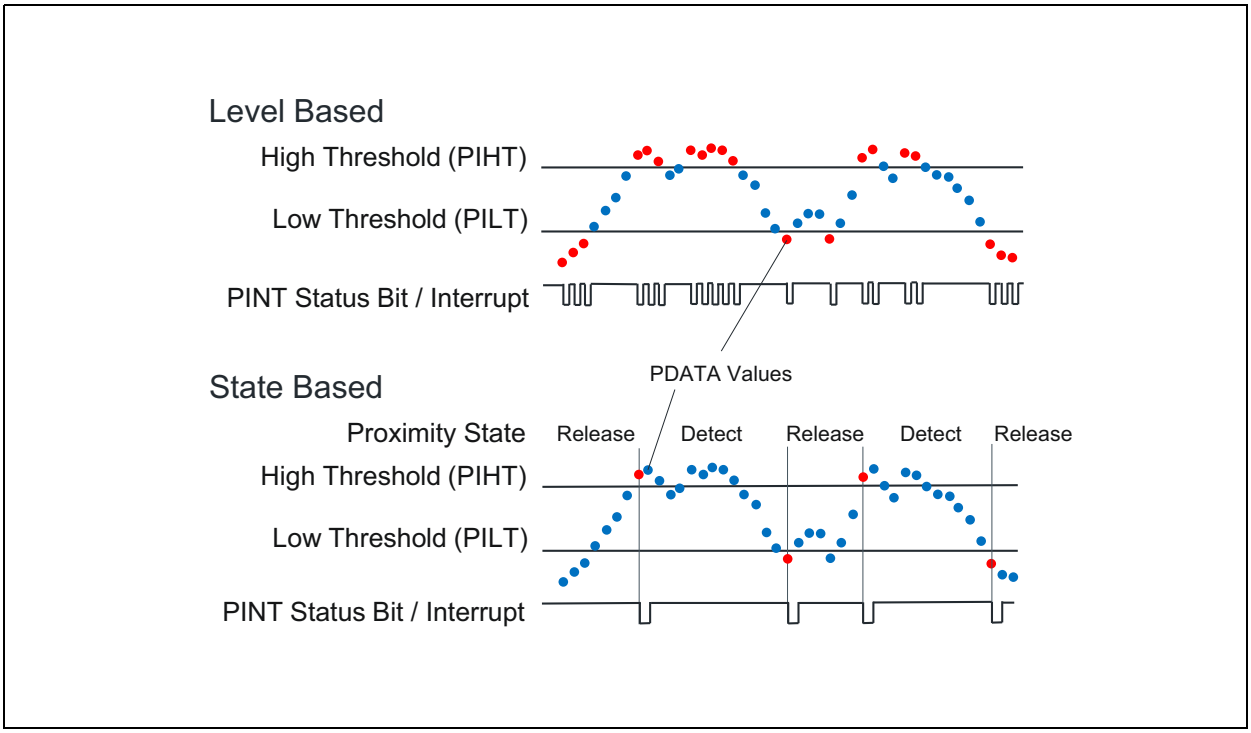
INTENAB Register (0xDD)

Figure 42:
INTENAB Register

Addr: 0xDD		INTENAB		
Bit	Bit Name	Default	Access	Bit Description
7:6	Reserved	00	RW	Reserved. Must be set to default value.
5	PIM	0	RW	Proximity Interrupt Mode 0 = Level based 1 = State based
4	PIEN	0	RW	Proximity Interrupt Enable
3	PSIEN	0	RW	Proximity Saturation Interrupt Enable
2	CIEN	0	RW	Calibration Interrupt Enable
1	ZIEN	0	RW	Zero Detect Interrupt Enable
0	Reserved	0	RW	Reserved. Must be set to default value.

The PIM (Proximity Interrupt Mode) bit selects the condition under which the PINT status bit and the corresponding interrupt (if enabled with PIEN) will be asserted.

Figure 43:
Proximity Interrupt Mode



FAC_L Register (0xE5)

Figure 44:
FAC_L Register

Addr: 0xE5		FAC_L		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Reserved	0x00 - 0xFF	R	Reserved for lot code data.

FAC_H Register (0xE6)

Figure 45:
FAC_H Register

Addr: 0xE6		FAC_H		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Reserved	0x00 - 0xFF	R	Reserved for lot code data.

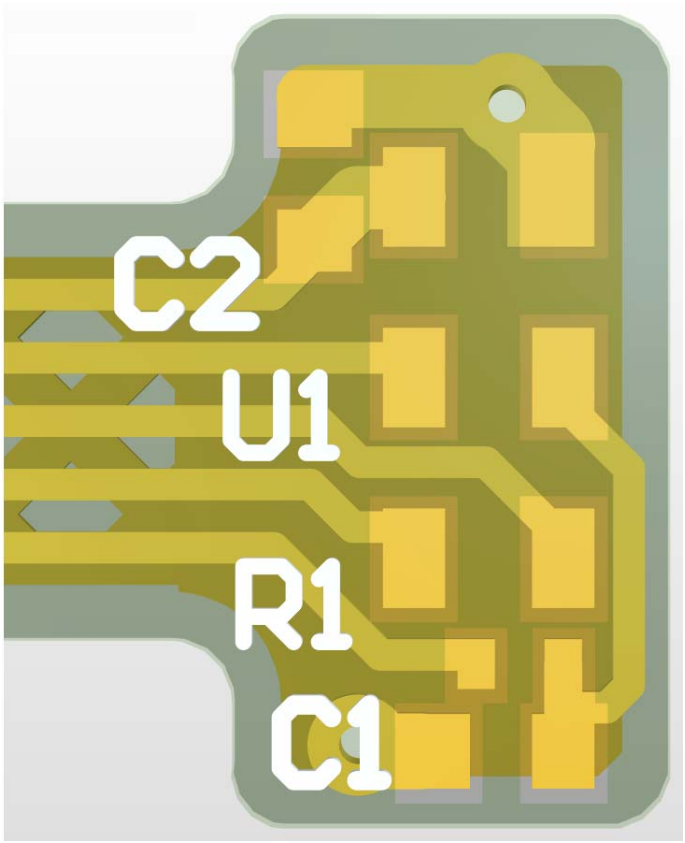
TEST9 Register (0xF9)

Figure 46:
TEST9 Register

Addr: 0xF9		TEST9		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Reserved	0x00	R/W	Reserved. Must be set to 0x07.

Application Information

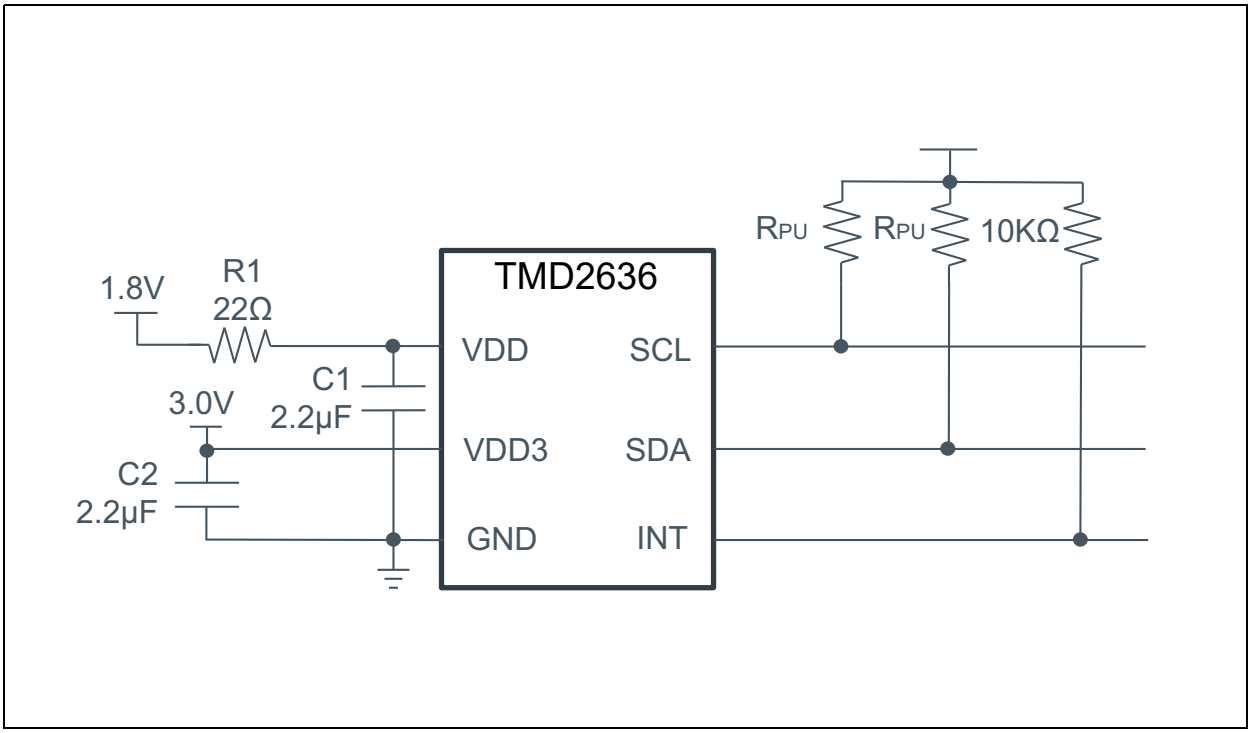
Figure 47:
Recommended Circuit Layout



Note(s):

1. The dominant factor governing device performance is the component placement, not necessarily component value. The placement of the decoupling capacitor, 2.2µF, is the most critical. Place the component on the same side of PCB as device as shown in the figure above. Make connection as close as possible to minimize series inductance and resistance. This is critical.

Figure 48:
Schematic



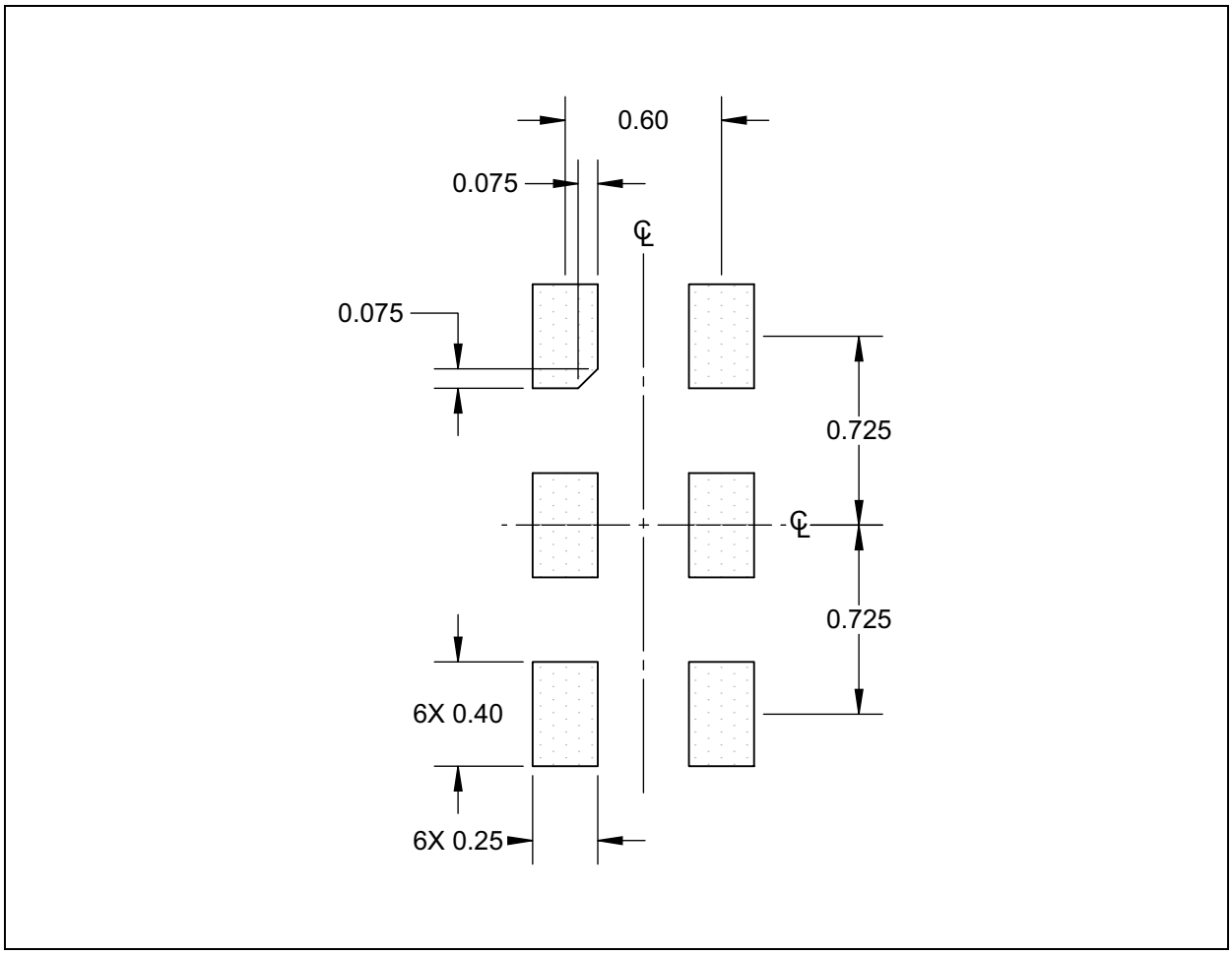
Note(s):

1. Place the C1 and C2 capacitors within 5mm of the module.
2. The value of the I^2C pull up resistors RPU should be based on the 1.8V bus voltage, system bus speed and trace capacitance.
3. C1 and C2 are critical components to protect the device during high voltage ESD strikes.
4. In systems subjected to high voltage ESD strikes, it is recommended to connect VDD to a host GPIO pin to allow the device to be independently power cycled.

PCB Pad Layout

Suggested PCB pad layout guidelines for the surface mount module are shown. Flash Gold is recommended as a surface finish for the landing pads

Figure 49:
Recommended PCB Pad Layout

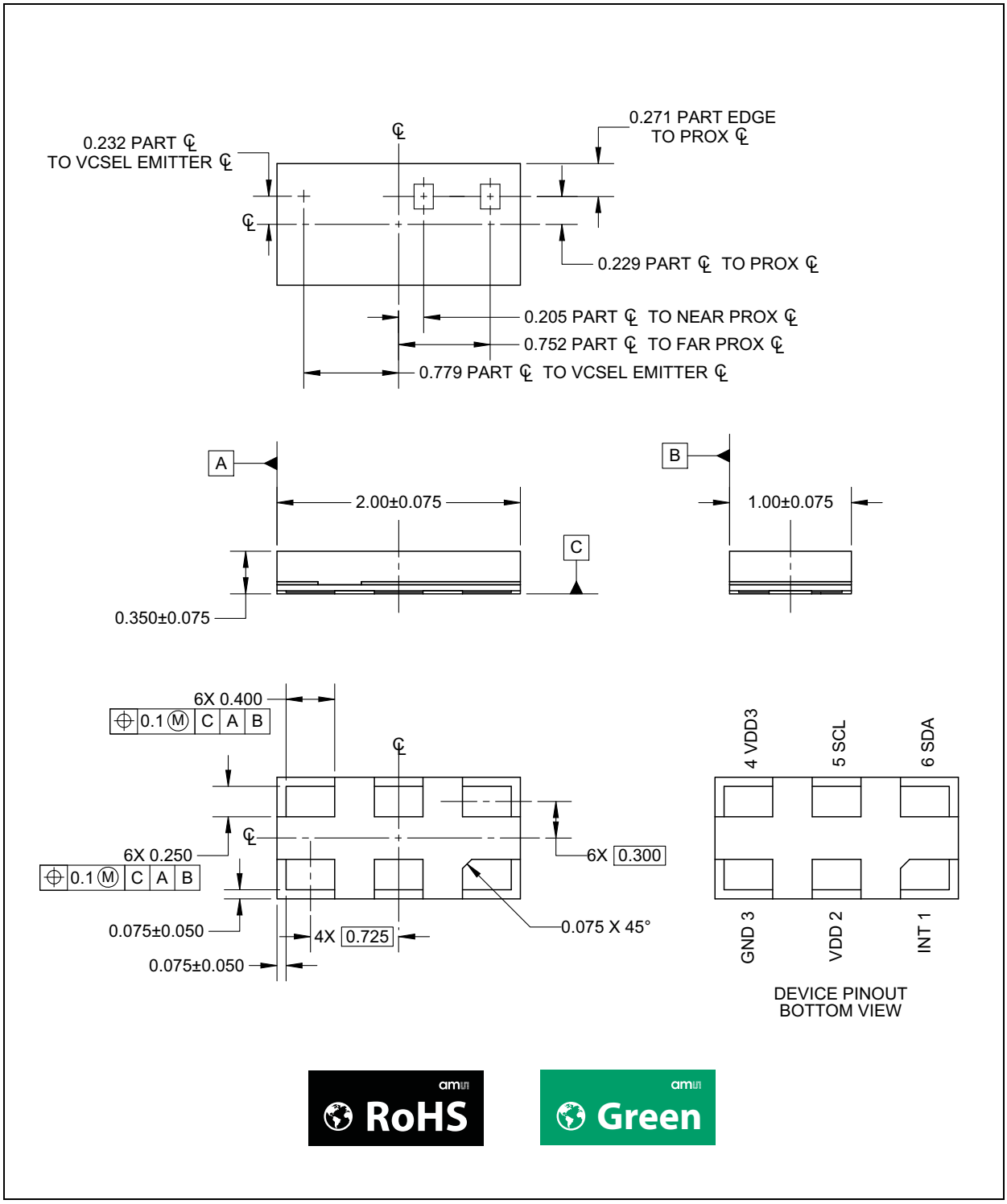


Note(s):

1. All linear dimensions are in millimeters.
2. Dimension tolerances are ±0.05mm unless otherwise noted.
3. This drawing is subject to change without notice.

Packaging Drawings

Figure 50:
TMD2636 Package Drawing

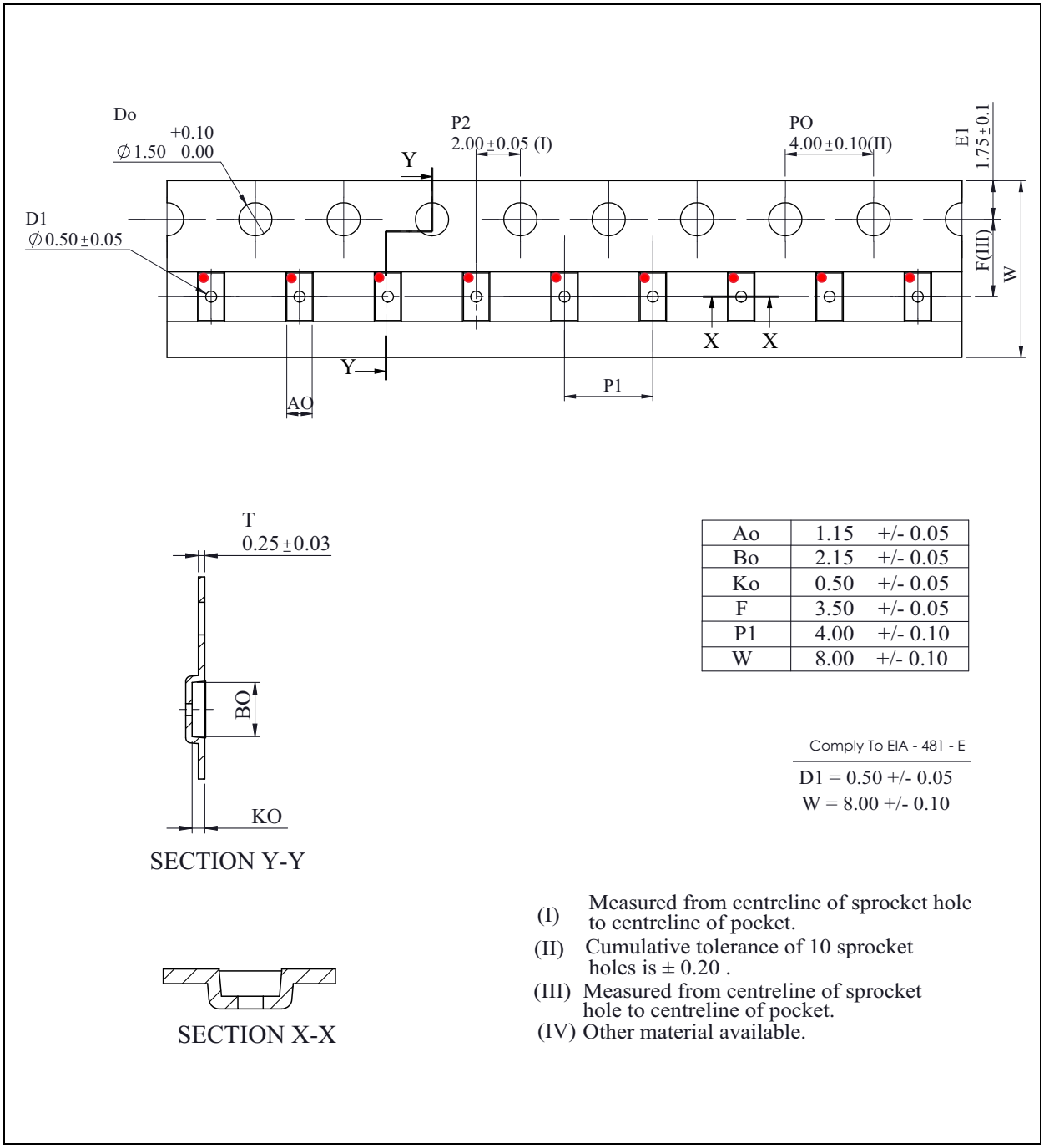


Note(s):

1. All linear dimensions are in millimeters.
2. Dimension tolerances are 0.05mm unless otherwise noted.
3. Contact finish is Au.
4. This package contains no lead (Pb).
5. This drawing is subject to change without notice.

Tape & Reel Information

Figure 51:
TMD2636 Tape & Reel Information



Ao	1.15	+/- 0.05
Bo	2.15	+/- 0.05
Ko	0.50	+/- 0.05
F	3.50	+/- 0.05
P1	4.00	+/- 0.10
W	8.00	+/- 0.10

Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ±0.10mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing A0, B0 and K0 are defined on ANSI EIA standard 481-B 2001.
4. **ams** packaging tape and reel conform to the requirements of EIA standard 481-B.
5. In accordance with EIA standard device pin 1 is located next to the sprocket holes in the tape.
6. This drawing is subject to change without notice.

Soldering & Storage Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

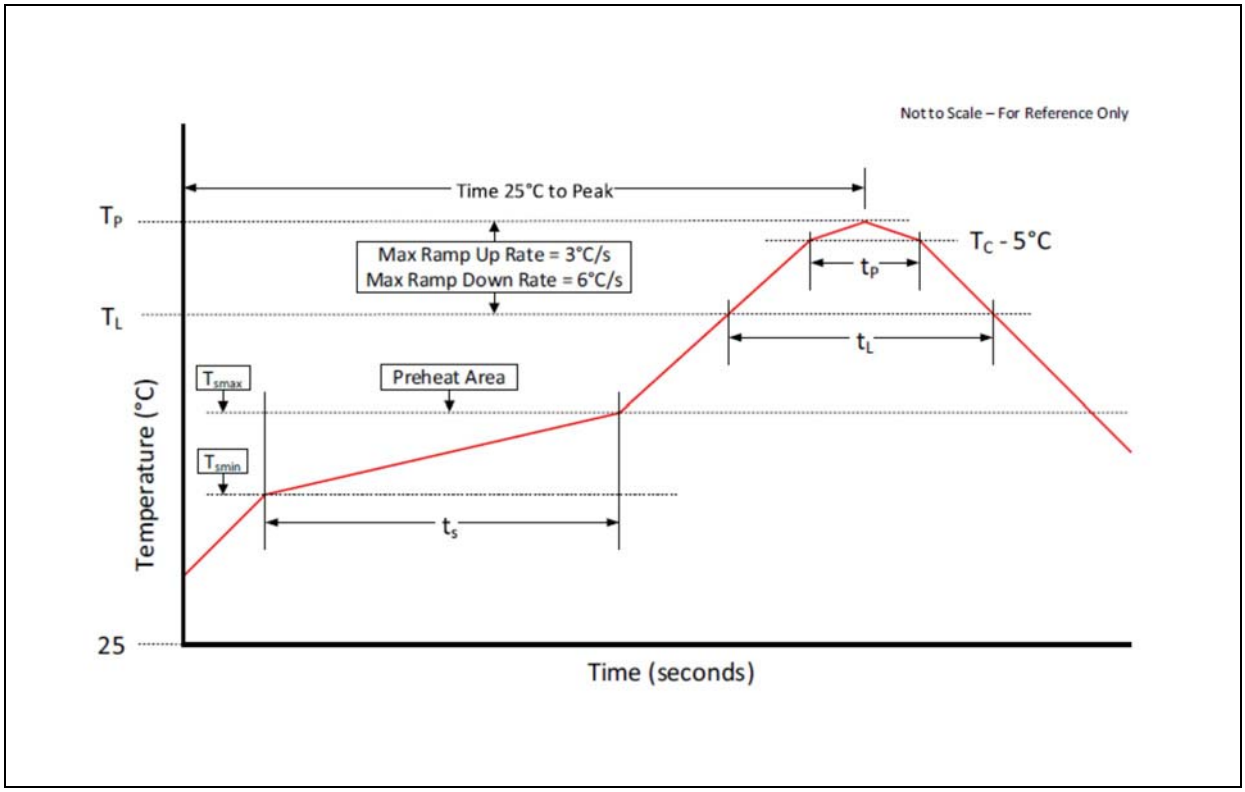
Figure 52:
Solder Reflow Profile

Profile Feature Preheat / Soak	Sn-Pb Eutectic Assembly	Pb- Free Assembly
Temperature Min (T_{smin})	100°C	150°C
Temperature Max (T_{smax})	150°C	200°C
Time (t_s) from (T_{smin} to T_{smax})	60 - 120 seconds	60 - 120 seconds
Ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183°C 60 - 150 seconds	217°C 60 - 150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the classification temp. of 235 °C. For suppliers T_P must equal or exceed the classification temp of 235°C.	For users T_P must not exceed the classification temp. of 260 °C. For suppliers T_P must equal or exceed the classification temp of 260°C.
Time (t_P) (1) within 5 °C of the specified classification temperature (T_c)	20 (1)	30 (1)
Ramp-down rate (T_P to T_L)	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note(s):

1. Tolerance for peak profile temperature (TP) is defined as a supplier minimum and a user maximum.

Figure 53:
Solder Reflow Profile Graph



Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 12 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 12 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 12 month shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

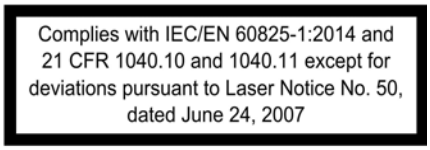
- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Laser Eye Safety



The TMD2636 is designed to meet the Class 1 laser safety limits including single faults in compliance with IEC/EN 60825-1:2014. In an end application system environment, the system may need to be tested to ensure it remains compliant. The system must not include any additional lens to concentrate the laser light or parameters set outside of the recommended operating conditions or any physical modification to the module during development could result in hazardous levels of radiation exposure.

Ordering & Contact Information

Figure 54:
Ordering Information

Ordering Code	I²C Bus	I²C Address	Delivery Form	Delivery Quantity
TMD26363	1.8V	0x39	Tape and Reel (13”)	10000 pcs/reel
TMD26363M	1.8V	0x39	Tape and Reel (7”)	1000 pcs/reel

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Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
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Revision Information

Changes from 1-01 (2020-Oct-21) to current revision 1-02 (2021-Feb-02)	Page
Removed “Confidential” from the footer	

Content Guide